

FM4442 256 Bytes Memory Card Chip

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Datasheet



Product Overview

Description

FM4442 is the memory card chip developed by Shanghai FM Co., Ltd. This chip has 256×8 Bits EEPROM with write protect function and programmable security code. With its contact configuration in accordance to ISO standard 7816 (synchronous transmission), FM4442 can be widely used in different types of IC memory cards.

Features

- 256×8-bits EEPROM organization;
- Byte-wise addressing
- 32×1-bit organization of protection memory
- Irreversible byte-wise write protection of lowest 32 addresses (Byte 0 ... 31)
- Two-wire link protocol
- End of processing indicated at data output
- Answer-to-Reset acc. to ISO standard 7816-3
- Data retention for minimum of ten years

- Programming time 2.5 ms per byte for both erasing and writing
- Contact configuration and serial interface in accordance with ISO standard 7816 (Synchronous transmission)
- Data can only be changed after entry of the correct 3-byte programmable security code (security memory)
- Compatible SLE4442

Pin Assignment

VCC C1 C6 GND

RST C2 C5 NC

CLK C3 C4 I/O

Pin Function

Pin	Symbol	Function
C1	VCC	Supply voltage 2.5V ~ 5V
C2	RST	Reset
C3	CLK	Clock input
C4	I/O	Bidirectional data line (open drain)
C5	NC	Not Connected
C6	GND	Ground



Function Description

The FM4442 consists of 256 x 8 bits EEPROM main memory and a 32-bit protection memory with PROM functionality. The main memory is erased and written byte by byte. Each of the first 32 bytes can be irreversibly protected against data change by writing the corresponding bit in the protection memory. Each data byte in this address range is assigned to one bit of the protection memory and has the same address as the data byte in the main memory which it is assigned to. Once written the protection bit cannot be erased (PROM).

Reset and Answer-to-Reset

Answer-to-Reset takes place according to ISO standard 7816-3 (ATR). The reset can be given at any time during operation. In the beginning, the address counter is set to zero together with a clock pulse and the first data bit (LSB) is output to I/O when RST is set from level H to level L. Under a continuous input of additional 31 clock pulses the contents of the first 4 EEPROM addresses is read out. The 33rd clock pulse switches I/O to high impedance Z and finishes the ATR procedure.

Answer-to-Reset	Byte1	Byte 2	Byte 3	Byte 4
(HEX)	DO ₇ DO ₀	DO ₁₅ DO ₈	DO ₂₃ DO ₁₆	DO ₃₁ DO ₂₄

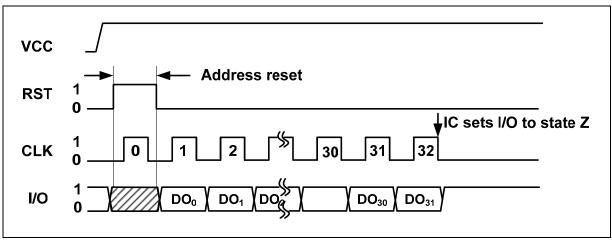


Figure 2 Reset and Answer-to-Reset



Commands

Commands Format:

MS				.SB	MSB Addi			dres	ress LSB			MSB [Da	Data LSB							
В7	В6	B5	B4	В3	B2	B1	B0	Α7	A6	A5	A4	А3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Command Introduction

(1) Read Main Memory

				Cor	trol				Address	Data
	В7	В6	B5	B4	В3	B2	B1	B0	A7A0	D7D0
Binary	0	0	1	1	Address	No effect				
Hexadecimal				30	00 _н FF _н	No effect				

The command reads out the contents of the main memory (with LSB first) starting at the given byte address (N = 0...255) up to the end of the memory. After the command entry the IFD has to supply sufficient clock pulses. The number of clocks is $m = (256 - N) \times 8 + 1$. The read access to the main memory is always possible.

(2) Read Protection Memory

				Cor	trol				Address	Data
	В7	B6	B5	B4	В3	B2	B1	B0	A7A0	D7D0
Binary	0	0	1	1	0	1	0	0	No effect	No effect
Hexadecimal				34	No effect	No effect				

The command transfers the protection bits under a continuous input of 32 clock pulses to the output. I/O is switched to high impedance Z by an additional pulse. The protection memory can always be read, and indicates the data bytes of the main memory protected against changing.

(3) Update Main Memory

				Cor	trol				Address	Data
	В7	В6	B5	B4	В3	B2	B1	В0	A7A0	D7D0
Binary	0	0	1	1	Address	Input data				
Hexadecimal				38	00 _н FF _н	Input data				

The command programs the addressed EEPROM byte with the data byte transmitted. Depending on the old and new data, one of the following sequences will take place during the processing mode:

- erase and write (5 ms) corresponding to m = 245 clock pulses
- write without erase (2.5 ms) corresponding to m = 124 clock pulses
- erase without write (2.5 ms) corresponding to m = 124 clock pulses (All values at 50 kHz clock rate.)



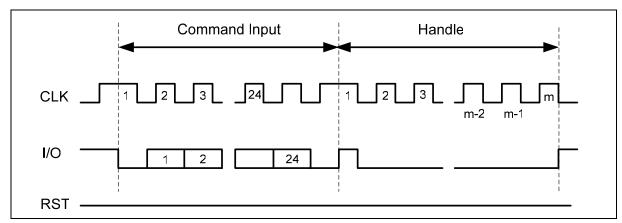


Figure 3 Update main memory

(4) Write Protection Memory

				Cor	trol				Address	Data
	B7	В6	B5	B4	В3	B2	B1	В0	A7A0	D7D0
Binary	0	0	1	1	1	1	0	0	Address	Input data
Hexadecimal				30	00 _н 1F _н	Input data				

The execution of this command contains a comparison of the entered data byte with the assigned byte in the EEPROM. In case of identity the protection bit is written thus making the data information unchangeable. If the data comparison results in data differences writing of the protection bit will be suppressed.

(5) Read Security Memory

				Cor	itrol				Address	Data
	B7	В6	B5	B4	В3	B2	B1	B0	A7A0	D7D0
Binary	0	0	1	1	No effect	No effect				
Hexadecimal				3	No effect	No effect				

Similar to the read command for the protection memory this command reads out the 4 bytes of the security memory.

(6) Update Security Memory

				Cor	ntrol				Address	Data
	B7	В6	B5	B4	В3	B2	B1	В0	A7A0	D7D0
Binary	0	0	1	1	1	0	0	1	Address	Input data
Hexadecimal				39	00 _н 1F _н	Input data				

Regarding the reference data bytes this command will only be executed if a PSC has been successfully verified before. Otherwise only each bit of the error counter (Address 0) can be written from "1" to "0". The execution times and the required clock pulses are the same as described under update main memory.



(7) Compare Verification Data

				Cor	ntrol				Address	Data
	B7	В6	B5	B4	В3	B2	B1	В0	A7A0	D7D0
Binary	0	0	1	1	0	0	1	1	Address	Input data
Hexadecimal				33	00 н03 н	Input data				

The command compares one byte of the entered verification data byte with the corresponding reference data byte.

PSC Verification

The FM4442 requires a correct verification of the Programmable Security Code PSC stored in the Security Memory for altering data if desired. The following table gives an overview of the necessary commands for the PSC verification. The sequence of the shaded commands is mandatory.

Command	Control	Address	Data	Remark
Command	B7B0	A7A0	D7D0	Nemark
Read security memory	31 _H	No effect	No effect	Check error counter
Update security memory	39 _H	00 _H	Input data	Write free bit in error counter input data: 0000 0ddd binary
Compare verification data	33 _H	01 _H	Input data	Reference data byte1
Compare verification data	33 _H	02 _H	Input data	Reference data byte2
Compare verification data	33 _H	03 _H	Input data	Reference data byte3
Update security memory	39 _H	00 _H	FF _H	Erase error counter
Read security memory	31 _H	No effect	No effect	Check error counter



Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply Voltage	V_{CC}	-0.3	-	6	V
Input voltage	V _i	-0.3	-	6	V
Storage temperature	T _{sto}	-25	-	+70	$^{\circ}$
Power dissipation	P _{tot}	-	-	70	mW

Operation Range

Parameter	Symbol	Min.	Тур.	Max.	Unit
Ambient temperature	T _A	-20	-	+60	$^{\circ}\mathbb{C}$
Supply Voltage	V_{CC}	2.5	5.0	5.5	V

DC Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit
Supply current	I _{cc}	-	3	10	mΑ
High level input voltage (I/O, CLK, RST)	V_{ih}	0.7 Vcc	-	Vcc	V
Low level input voltage (I/O, CLK, RST)	V _{il}	0	-	0.3* Vcc	V
High level input current (I/O, CLK, RST)	l _h	-	-	50	μA
Low level output current (V _{OL} = 0.4V, open drain)	l _{ol}	1	-	-	mΑ
High level output current (V _{OH} = 5V, open drain)	I _{oh}	-	-	50	μA
Input capacitance	Ci	-	-	10	pF

AC Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit
CLK Frequency f _{CLK}	f_{CLK}	7		50	kHz
I/O High time (Start Condition)	t ₁	10			μs
CLK High to I/O Hold time	t_2	4			μs
I/O Low to CLK Hold time (Start Condition)	t_3	4			μs
I/O Setup to CLK High time	t_4	1			μs
CLK Low to I/O Hold time	t ₅	1			μs
CLK High to I/O Clear time (Stop Condition)	t ₆	4			μs
CLK Low to I/O Valid time	t ₇			2.5	μs
CLK Low to I/O Valid time	t ₈			2.5	μs
CLK Low to I/O Clear time	t ₉			2.5	μs
RST High to CLK Setup time	t ₁₀	4			μs
CLK Low to RST Hold time	t ₁₁	4			μs
RST High time (address reset) time	t ₁₂	20	50		μs
RST Low to I/O Valid time	t ₁₃			2.5	μs
RST Low to CLK Setup time	t ₁₄	4			μs



Parameter	Symbol	Min.	Тур.	Max.	Unit
CLK High time	t ₁₅	9			μs
CLK Low time	t ₁₆	9			μs
CLK Low to I/O Valid time	t ₁₇			2.5	μs
Reset time for Break	t ₁₈	5			μs
RST High to I/O Clear time (Break)	t ₁₉	2.5			μs
CLK Rise time	t _R			1	μs
CLK Fall time	t _F			1	μs
Erase time	t _{ER}	2.5@ f _{CLK} = 50kHz			ms
Write time	t _{WR}	2.5@ f _{CLK} = 50kHz			ms
Power on reset time				100	μs

Timing Diagrams

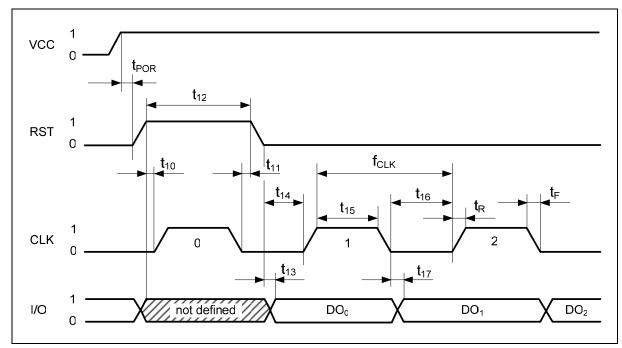


Figure 4 FM4442 Reset and Answer-to-Reset

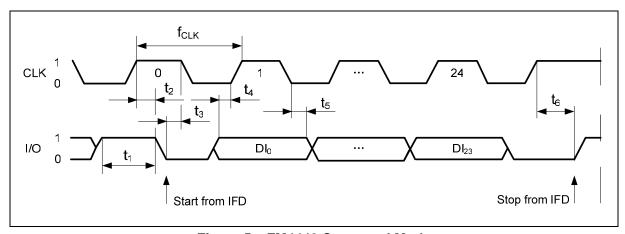


Figure 5 FM4442 Command Mode

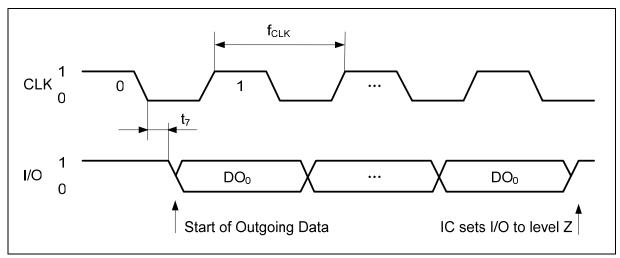


Figure 6 FM4442 Outgoing Data Mode

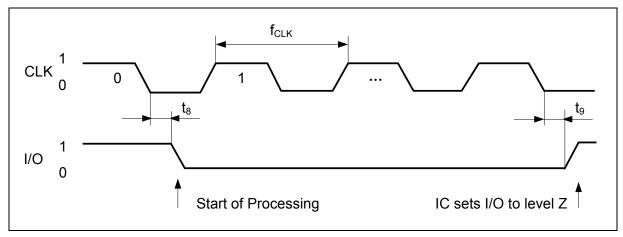


Figure 7 FM4442 Processing Mode

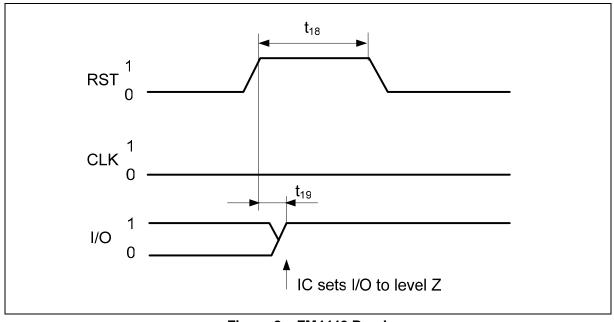


Figure 8 FM4442 Break



Ordering Information

Ordering Code	Package	Product Carrier	Operation Range
FM4442-P5-R	Micro-Module Package (6Pin)	Reel	-20°C ~ +60°C
FM4442-M3-R	Micro-Module Package (6Pin)	Reel	-20 C * 100 C



Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Oct. 2007	10		Initial Release.
1.1	May. 2008	11	Sales and service	Updated the address of HK office.
2.0	Aug. 2008	13		Updated "Description"、"Electrical Characteristics" and "Ordering information".
3.0	Dec. 2008	13	Sales and service	Updated the address of Beijing office.



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